



diablo
technologies™

Kevin M Wagner
Jerome McFarland

Vice President, Marketing
Principal Product Marketer

PROBLEM SOLVED.

Diablo Technologies Confidential

All Information In This Deck Under Embargo Until August 6

Company Update

MEMORY CHANNEL STORAGE™
FLASH MEMORY SUMMIT 2014 UPDATE

UPDATE ON Diablo Technologies

COMPANY UPDATE

Diablo Growth

- + **More than doubled in size by employees in one year**
 - + From 30 to 90+ employees
 - + Strong growth trend continuing in North America and around world
 - + Growth in all areas of the company

Diablo Expansion

- + **Opened Silicon Valley office August 1, 2014**
 - + Sales, Marketing, engineering
- + **Expansion driven by strong customer traction and MCS interest**



Carbon₁ Update

MEMORY CHANNEL STORAGE™
FLASH MEMORY SUMMIT 2014 UPDATE

UPDATE ON MCS™ FIRST GENERATION (Carbon₁) SUPERMICRO ANNOUNCEMENT

Diablo Forges Strategic Partnership with Supermicro

- + **Supermicro X9-series platforms to be enabled with MCS via SanDisk™ ULLtraDIMM™**
- + Strong lineup of Supermicro platforms including twin architecture, GPU Compute, SuperStorage and Hyper-Speed HFT platforms
- + Diablo, SanDisk and Supermicro to jointly target:
 - Datacenter
 - Cloud Computing
 - Virtualization
 - Financial Services
 - HPC Applications
- + **Future collaboration on technology**
 - + Supermicro to provide input/feedback on future technologies and architectures
- + **Boston Group (leading Supermicro VAR) already announced support for MCS on SMC**



UPDATE ON MCS™ FIRST GENERATION (Carbon₁) TECHNOLOGY UPDATE

US Patent and Trademark Office issued patent to Diablo for MCS

- + **First patent issued by USPTO for interfacing co-processors and I/O for DDR3 memory systems**
 - + Connects non-volatile memory directly to CPU memory controllers
 - + Learning machine for interleaving/de-interleaving and scrambling/de-scrambling of data
 - + Method for remapping non-linear DIMM address space into driver address space
- + **Enhances company technology and growth**
 - + Expands Diablo's current patent and IP portfolio

Carbon₂ Introduction

MEMORY CHANNEL STORAGE™
FLASH MEMORY SUMMIT 2014 UPDATE

MCS™ SECOND GENERATION (Carbon₂) INTRODUCTION

Second Generation Design Goal

- + **Fast Time-to-Market & performance, functionality improvements**

Enhancements

- + **DDR4 memory interface**
 - + Modular design allows low risk move to new interfaces
- + **NanoCommit™ Technology**
 - + API that allows DRAM persistence on nanosecond timescale to terabytes of flash memory
- + **MCS Processing Engine Enhancements**
 - + Optimized processing capabilities with increased performance
 - + Firmware changes for increased functionality, performance
 - + NanoCommit is first example, several others planned
 - + Reduced latency even further (even lower than 3.3 microseconds!)

MCS™ SECOND GENERATION (Carbon₂) REFERENCE DESIGN KIT

Phase 1: MDK2 Development Kit

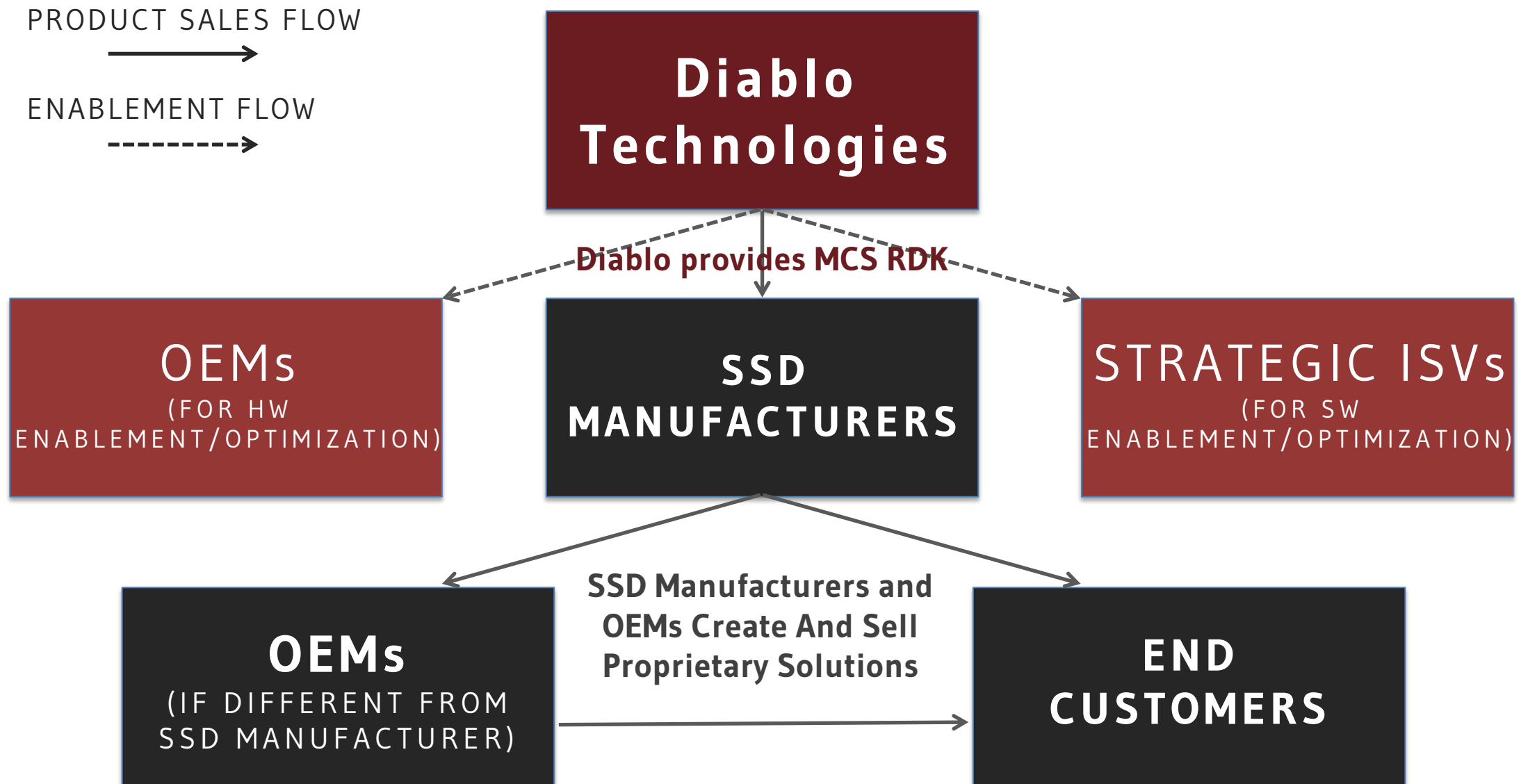
- + **FPGA based design**
- + **Early prototyping**
- + **UEFI, firmware, driver development**

Phase 2: Carbon₂ Reference Design Kit

- + **ASIC based reference design**
- + **Full reference storage subsystem (further announcements to come)**
- + **Linux, VMware, MS Windows drivers**
- + **Ecosystem enablement**
 - + OEM Prequalifications
 - + ISV testing/optimizations, proof points
 - + Media architectural reviews



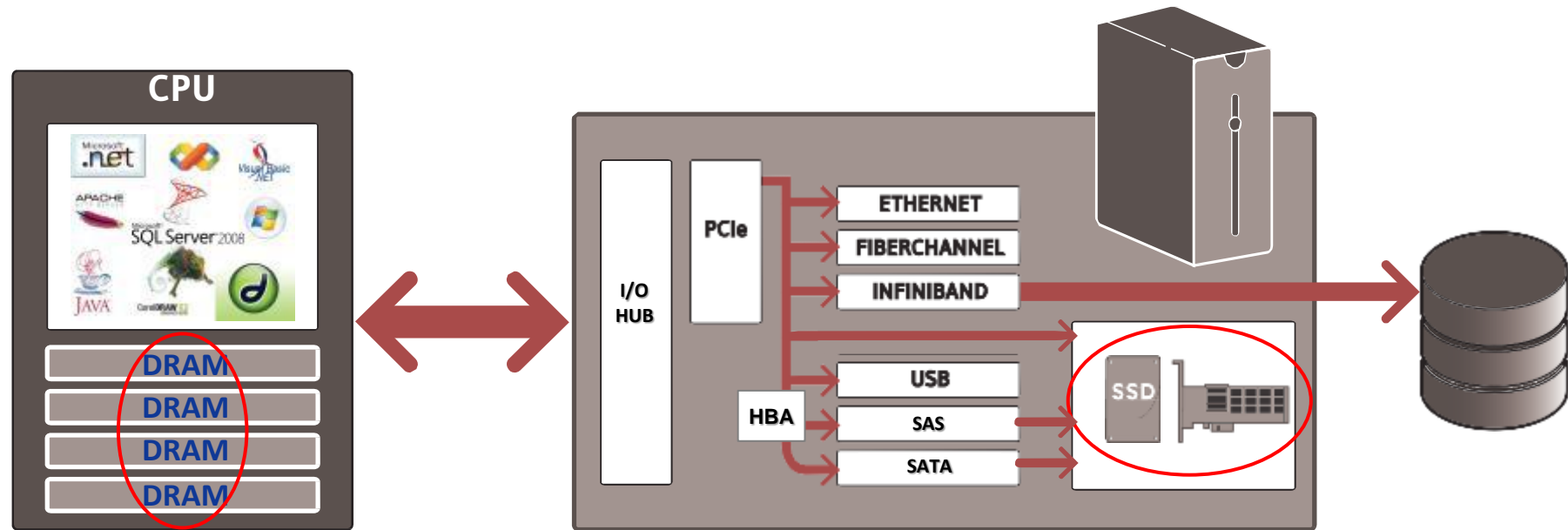
MEMORY CHANNEL STORAGE ECOSYSTEM



NanoCommit™ Technology Introduction

MEMORY CHANNEL STORAGE™
FLASH MEMORY SUMMIT 2014 UPDATE

Historically: DRAM isolated from persistent memory



Memory Segregation

- + DRAM closely coupled with CPU
- + Flash accessed via I/O subsystem
- + Creates significant gap between dynamic memory and persistent storage

NanoCommit

MEMORY SEGREGATION CONSEQUENCES

Example: Database Performance Considerations

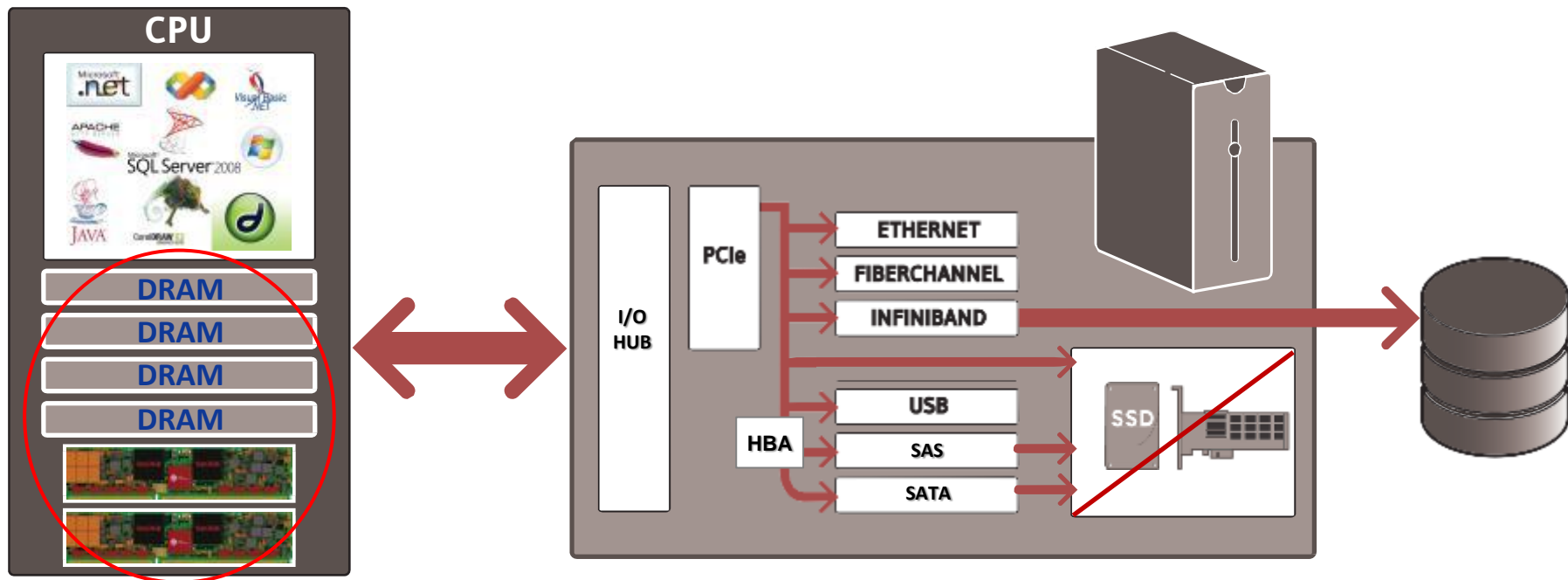
	Flash-Backed DRAM	SSDs (PCIe/SAS/SATA)
"Memory Speed" Data Persistence (Transaction Logging)	✓	✗
Transaction Granularity (Transaction Logging)	✓	✗
Mixed-Workload Performance (General Purpose Acceleration)	✓	✓
Storage Capacity (General Purpose Acceleration)	✗	✓
\$/GB (All)	✗	✓

Segregated Architectures Fall Short

+ Tradeoffs between solution complexity, performance and cost

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DRAM AND FLASH CO-LOCATED WITH MCS



Memory Convergence (Proximity)

- + Both DRAM and Flash within memory subsystem
- + Lowest Flash latency
- + Terabytes of storage on Memory Channel Interface

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NEXT STEP: TREAT ALL MEMORY LIKE MEMORY

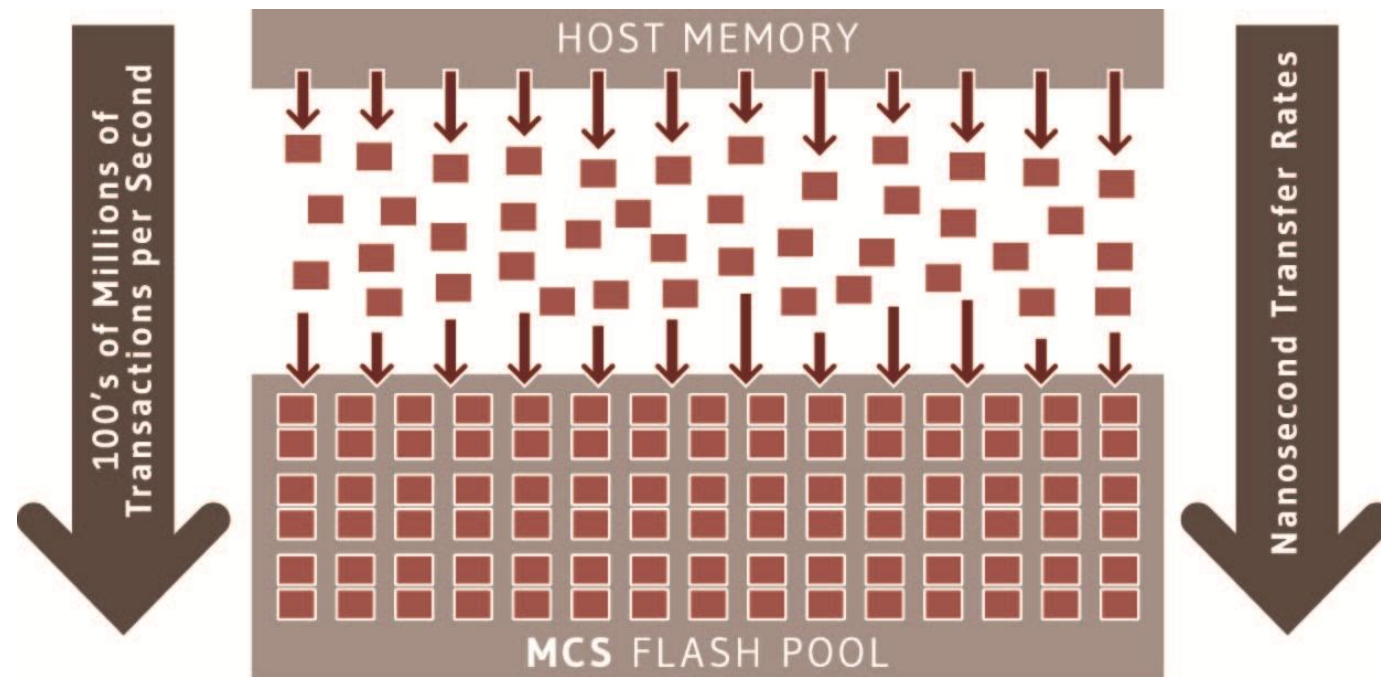


Memory Convergence (Access)

- + Treat Flash more like DRAM
- + Access with increased granularity and speed
- + Gap between dynamic memory and persistent storage significantly diminished

NanoCommit

THE ENABLING TECHNOLOGY



What NanoCommit™ Does

- + Performs small writes to Flash with high transaction rates
- + Enables mirroring of DRAM to persistent storage

NanoCommit

MCS WITH NANOCOMMIT: A UNIFYING SOLUTION

Example: Database Performance Considerations

	Flash-Backed DRAM	SSDs (PCIe/SAS/SATA)	MCS With NanoCommit
"Memory Speed" Data Persistence (Transaction Logging)	✓	✗	✓
Transaction Granularity (Transaction Logging)	✓	✗	✓
Mixed-Workload Performance (General Purpose Acceleration)	✓	✓	✓
Storage Capacity (General Purpose Acceleration)	✗	✓	✓
\$/GB (All)	✗	✓	✓

Converged Memory = Improved Performance And Reduced Complexity

NanoCommit

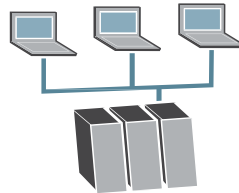
IT'S ALL ABOUT THE APPLICATIONS



**DATABASE/
HYPERSCALE**



**ULTRA-LOW
LATENCY APPLICATIONS**



**VIRTUAL
DESKTOPS**



**BIG DATA
ANALYTICS**



**SERVER
VIRTUALIZATION**



Thank You!



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FOLLOW-UP

For Any Questions:

- + **JPR Communications**
 - + Dan Miller
 - + (818) 884-8282 ext. 13
 - + dan@jprcom.com

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