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WHITE PAPER

NOISE DAMPING TECHNIQUES FOR SOLID-STATE STORAGE IN MILITARY-EMBEDDED SYSTEMS

KEY FACTORS IN UNDERSTANDING COMMON SIGNAL INTEGRITY ISSUES

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DOCUMENT: SSWP00-NOISEDAMPSOLSTSTORAGEMILEMBSYS-R

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INTRODUCTION

Parallel ATA (PATA) has been the dominant storage interface in embedded systems for some time. The use of solid-state storage is a common solution for embedded systems because of its small form factor, reliability, and ability to endure harsh environmental conditions.

As the support advances for more sophisticated and higher performing interfaces, the proper design techniques must be applied to assure that signal integrity is maintained in minimizing potential problems, both initially and over the life of the product.

This white paper describes the key factors in understanding the common signal integrity issues associated while interfacing to solid-state storage in embedded systems, and gives some real-world examples. This white paper also describes the storage interfaces that are in store for future embedded systems and the associated design challenges.

BACKGROUND

Signal integrity problems arise from the physical nature of the interconnecting wires. A wire is not the same as a connection line on a schematic. A real wire has resistance, capacitance to ground and to other wires, and inductance. At higher frequencies, the capacitance and inductance cause the wire to act like a transmission line, and antenna effects can cause crosstalk and electromagnetic interference (EMI).

FACTORS OF SIGNAL INTEGRITY ISSUES

The following section provides some definitions of factors leading to signal integrity issues and the resultant problems that may occur.

RINGING

Ringing is an unwanted oscillation in a circuit, generally caused when an electrical pulse causes the parasitic inductances and capacitances in the circuit to resonate at their characteristic frequency. This is similar to an overshoot condition.

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POOR OR NOISY GROUNDING

Lack of a proper ground plane technique can result in poor or noisy grounding in systems. Poor or noisy grounding can lead to false signal triggering, unstable timing, and the latching of erroneous data and address signals.

GROUND BOUNCE

Ground bounce is a phenomenon associated with transistor switching where the gate voltage can appear to be less than the local ground potential, causing unstable operation of the logic gate. Similar to poor or noisy grounding, ground bounce can lead to false signal triggering, unstable timing, and the latching of erroneous data and address signals.

SKEW

Skew is the difference in the total propagation delay between two signals as the signals transit the bus. Too much skew can result in improper latching of erroneous address or data signals. Large skews, which occur by not following the proper PCB trace specifications, can result in timing problems and the latching of erroneous data and address signals.

SLEW RATE

Slew rate is the rate of the signal change in transition from low-to-high or high-to-low. The slew rate is defined by the interface specification and is related to the impedance of the signal. The slew rate of signals that overshoot are steep, and the slew rate of signals that are over-damped are flat.

CROSSTALK

Crosstalk is the unwanted capacitive or inductive coupling from one signal that causes an unwanted effect in another signal, typically caused by improper grounding or not following proper PCB trace guidelines. Crosstalk can result in latching of erroneous address or data signals.

TERMINATION

Termination is the need to put a resistor or resistor-capacitor network on a transmission line to prevent signal reflections due to the impedance mismatch between devices. Improper termination can result in overshoots, over-damping, and signal reflections.

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OVERSHOOTS

Overshoots have steep slew rates and can be dangerous in that they can cause device failures over time on a rising edge and ground bounce on a falling edge. Each time an overshoot occurs on a rising edge, protection diodes turn on, and silicon junctions within the ICs (drivers and receivers) are stressed. If these stresses are large and repeated frequently, the product eventually fails, often in the field rather than during manufacturing testing. An undershoot, which typically occurs after the overshoot, can lead to false logic level triggering.

OVER-DAMPING

Over-damping has a more flattened slew rate and can lead to violations of setup and hold times because the threshold levels are more drawn out.

RISE TIME

The rise time is the time required for a signal to change from a specified low value to a specified high value. Typically, these values are 10% to 90% of the step height.

PROPAGATION DELAY

Propagation delay is the amount of time required for an input signal at one part of the system to become stable and valid at another part of the system.

DESIGN CONSIDERATIONS WITH THE PATA INTERFACE

Designing in current ATA solutions to interface to solid-state storage subsystems can be straight forward. Chipsets made by Intel, AMD/ATI, Via Technologies, Ali (Acer Labs), and SiS (Silicon Integrated Systems) are proven and well-tested designs. These chipsets have a lot of information available, such as reference designs, schematics, layouts, thermal and mechanical guidelines, and drivers that can be easily integrated and implemented into a design.

However, the chipsets may be costly and overkill for the application. In addition, the chipsets may take up too much board space for designs that are real estate limited. In these cases, one may choose to develop their own ATA interface such as with an FPGA. Careful consideration must be made

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in development of a proper ATA interface solution. The following sections provide some design rules from the ATA specifications. The following table shows the required signal types and termination for the ATA signals.

Table 1: Driver Types And Required Termination

Signal	Source	Type	Host	Device
RESET#	Host	TP	-	-
DD(15:0)	BiDir	TS	10K PD on DD7	-
DMARQ	Device	TS	5.6K PD	-
DIOR#: HDMARDY#: HSTROBE	Host	TS	-	-
DIOW#	Host	TS	-	-
IORDY: DDMARDY#: DSTROBE	Device	TS	4.7K PU	-
CSEL	Host	TS	GND	10k PU
DMACK#	Host	TP	-	-
INTRQ	Device	TS	10K PD or PU	-
DA(2:0)	Host	TP	-	-
PDIAG#	Device	TS	-	10K PU
CS0#, CS1#	Host	TP	-	-
DASP#	Device	OC	-	10K PU

Note: TP = Totem Pole, TS = Tri-State, OC = Open Collector, PU = Pull Up, PD = Pull Down

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The following table lists the additional design requirements that are essential when supporting Ultra DMA (UDMA) modes.

Table 2: Series Termination Requirements for UDMA

Signal	Host Termination	Device Termination
RESET#	33Ω	82Ω
DD(15:0)	33Ω	33Ω
DMARQ	82Ω	22Ω
DIOR#: HDMARDY#: HSTROBE	22Ω	82Ω
DIOW#	22Ω	82Ω
IORDY: DDMARDY#: DSTROBE	82Ω	22Ω
DMACK#	22Ω	82Ω
INTRQ	82Ω	22Ω
DA(2:0)	33Ω	82Ω
CS0#, CS1#	33Ω	82Ω

Table 3: DC Characteristics

Item	Up to UDMA Mode 4		Greater than UDMA Mode 4	
	Min.	Max.	Min.	Max.
Edge Slew Rate	-	1.25V/ns	0.4V/ns	1.0V/ns
Signal Capacitance	-	20pf	-	17pf

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Per the ATA specifications:

"*Hosts that support Ultra DMA transfer modes greater than 2 shall not share signals between primary and secondary I/O ports. They shall provide separate drivers and receivers for each cable.*"

Per the ATA specifications, there are PCB trace requirements for UDMA as well:

"'*The longest DD(15:0) trace shall be no more than 0.5" longer than either STROBE trace as measures from the IC pin to the connector. The shortest DD(15:0) trace shall be no more than 0.5" shorter than either STROBE trace as measured from the IC pin to the connector.*'"

Also per the ATA specifications, there are requirements if a cable is used:

"Either a single device direct connection configuration or an 80-conductor cable connection configuration shall be used for systems operating with UDMA modes greater than 2. An 80 conductor cable assembly differs from a 40 conductor cable in that it adds 40 ground lines to the cable between the 40 signal lines defined for the 40 conductor assembly. These added ground lines are connected inside each connector on the cable assembly to the seven ground pins defined for the 40 conductor assembly This results in a lower impedance and greatly reduced crosstalk for signals on the data bus as well as a much improved behavior of electrical signals on the bus."

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EXAMPLES

The following section provides examples of some systems with signal integrity issues:.

OVERSHOOT AND OVER-DAMPING

Figure 1 shows a scope shot of the two Chip Select signals (CS0 and CS1) that should be identical in timing. There is no series termination on CS0 and 100Ω on CS1. The results are some overshoot on the CS0 signal and some over-damping on the CS1 signal.

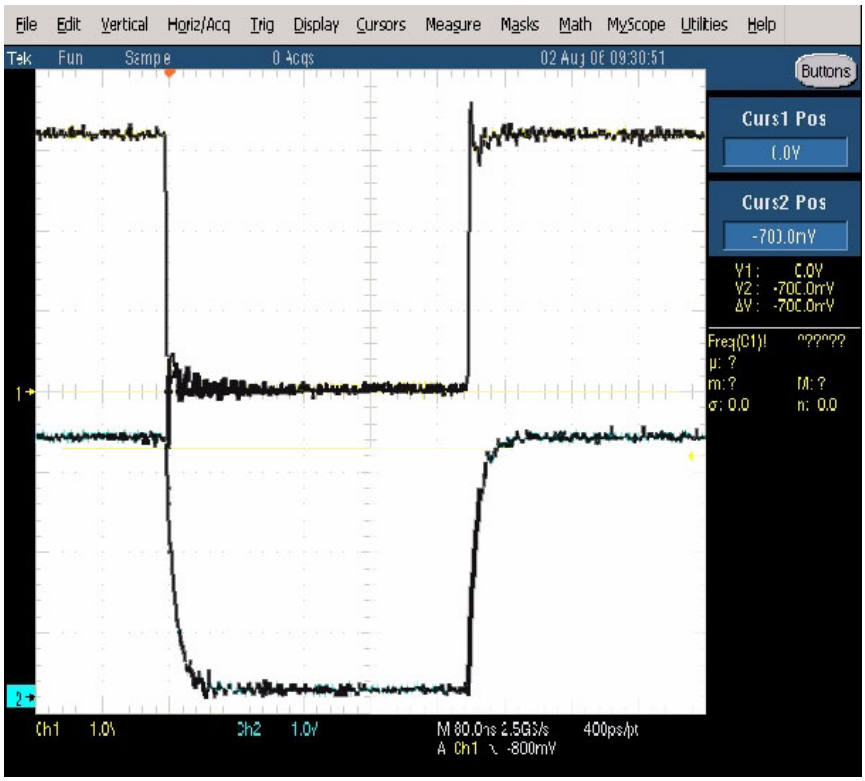

Figure 1: Overshoot of CS0, Over-Damping of CS1

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RISE TIME/GROUND NOISE AND FALSE TRIGGERING

Figure 2 shows the same Chip Select signals when linked to the Logic Analyzer. Note the false logic level occurring on the CS1# signal due to the slow rise time or possibly a noisy ground during the transition period. This is a great example of two seemingly identical signals behaving differently because of the impedance mismatch.

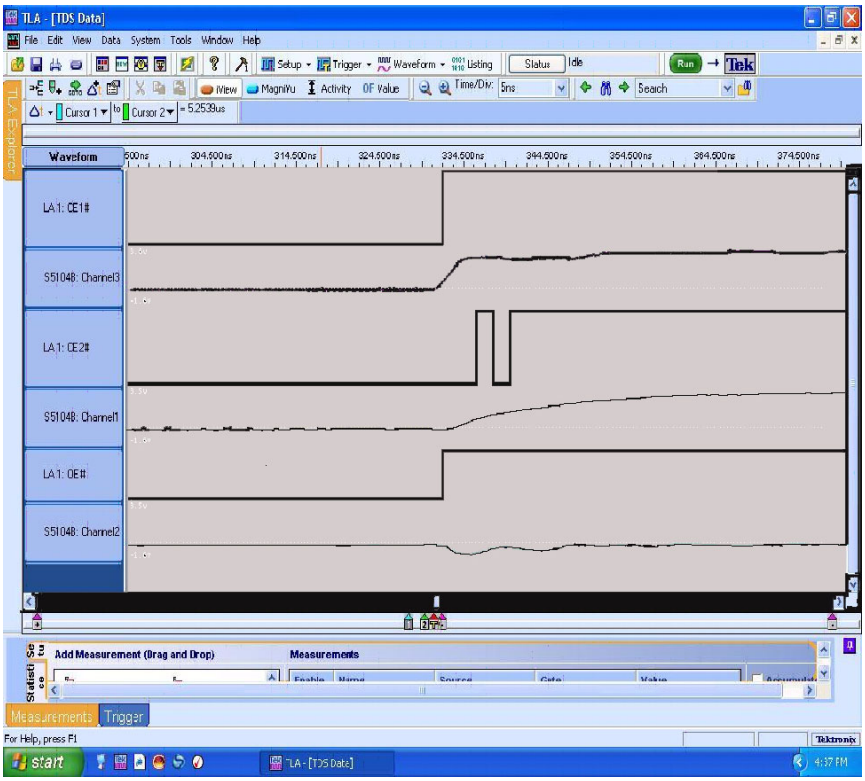

Figure 2: Same CS0 and CS1 Signals on the Logic Analyzer

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RINGING/OVERSHOOT AND GROUND BOUNCE

Figure 3 shows a Chip Select signal (CS0) with respect to a Data line (D4). Note the overshoots below ground (-600mV) on the signals and the corresponding ground bounce absorbed into the D4 signal. Also note the undershoot to 380mV on the D4 line. A value above 0.8V would violate the VIL specification.

Figure 3: CS0 and D4 Causing Ground Bounce

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POWER SUPPLY NOISE

Power supply noise can cause permanent damage if the noise exceeds the input voltage requirements of the storage subsystem. In addition, power supply noise can effect the proper operation of the storage subsystem itself such as the writing or reading of invalid data, sector corruption, and so on. Although the power supply seemed clean after the preliminary inspection, the following figure shows an anomaly that was found after monitoring the system power supply for several days.

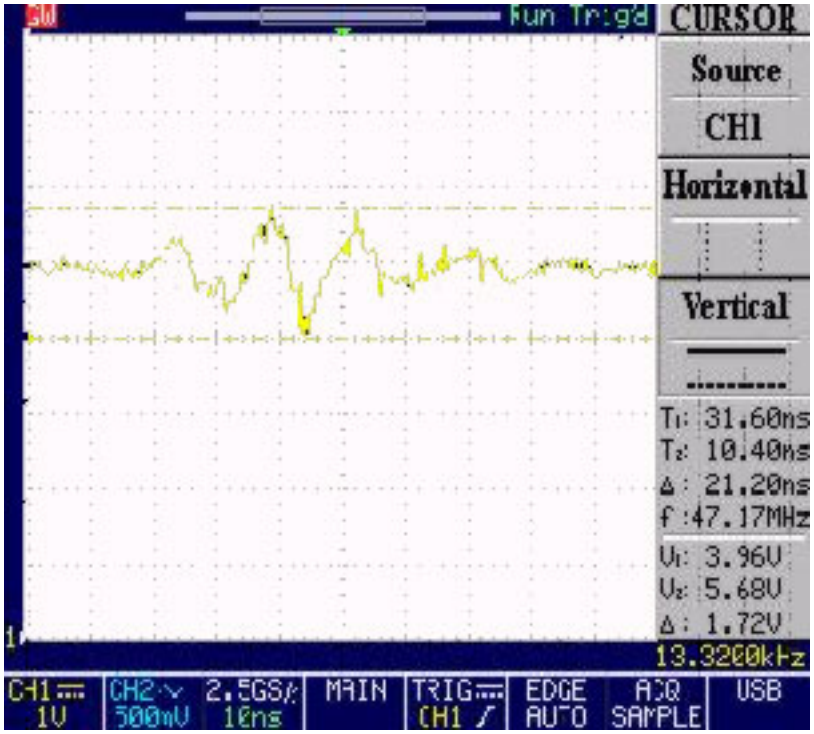

Figure 4: Example of Power Supply Noise

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SHARED BUS ARCHITECTURE

Sharing a bus is a method in allocating common signals across multiple devices for purpose of saving board space, device pins, and so on. Shared bus architecture is a common method, but careful timing considerations must be made as to not violate the ATA specification. In addition, the UDMA specification clearly states that the host should not share signals between primary and secondary IDE ports.

The following figure shows a standard type IDE configuration that has dedicated address/data busses and control lines for each IDE port.

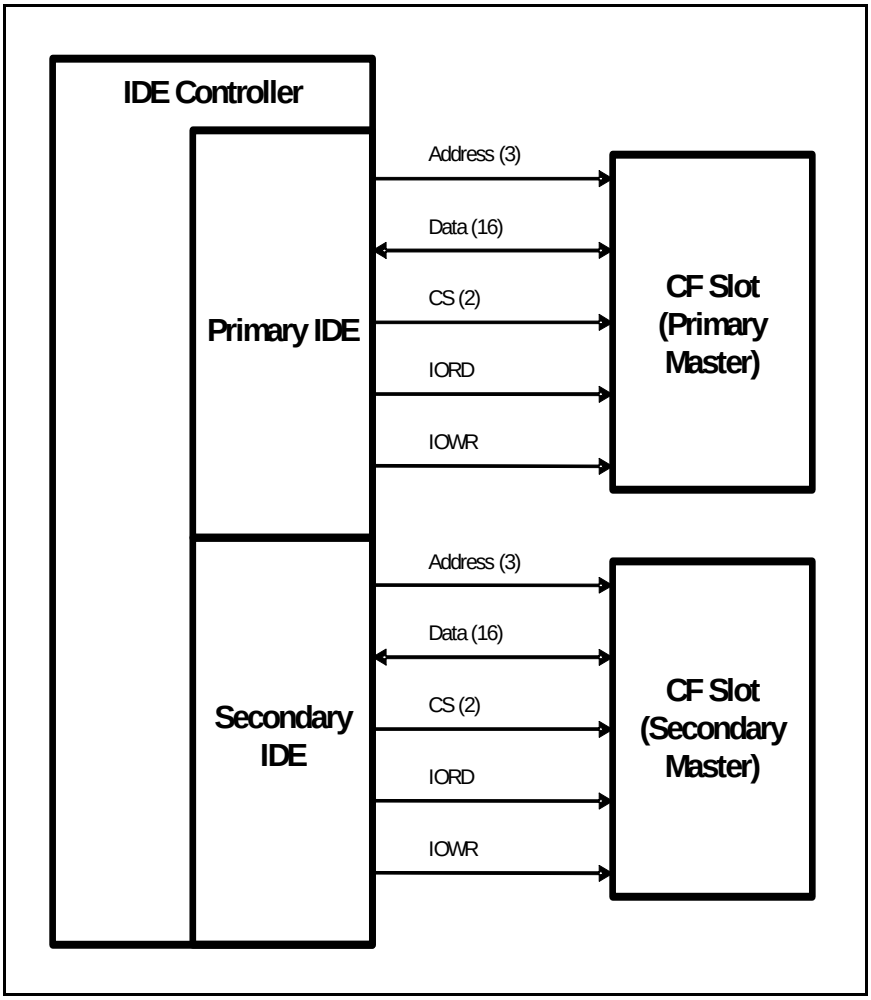

Figure 5: Standard IDE Controller Configuration

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Figure 6 shows a common shared bus architecture system for storage. The address/data bus and read/write enable lines are shared, but the chip select signals are isolated so that the IDE controller has capability of choosing the proper CF slot to read/write to. Common problems arise when the IORD or IOWR violate their setup and hold times when toggling reads or writes between IDE ports.

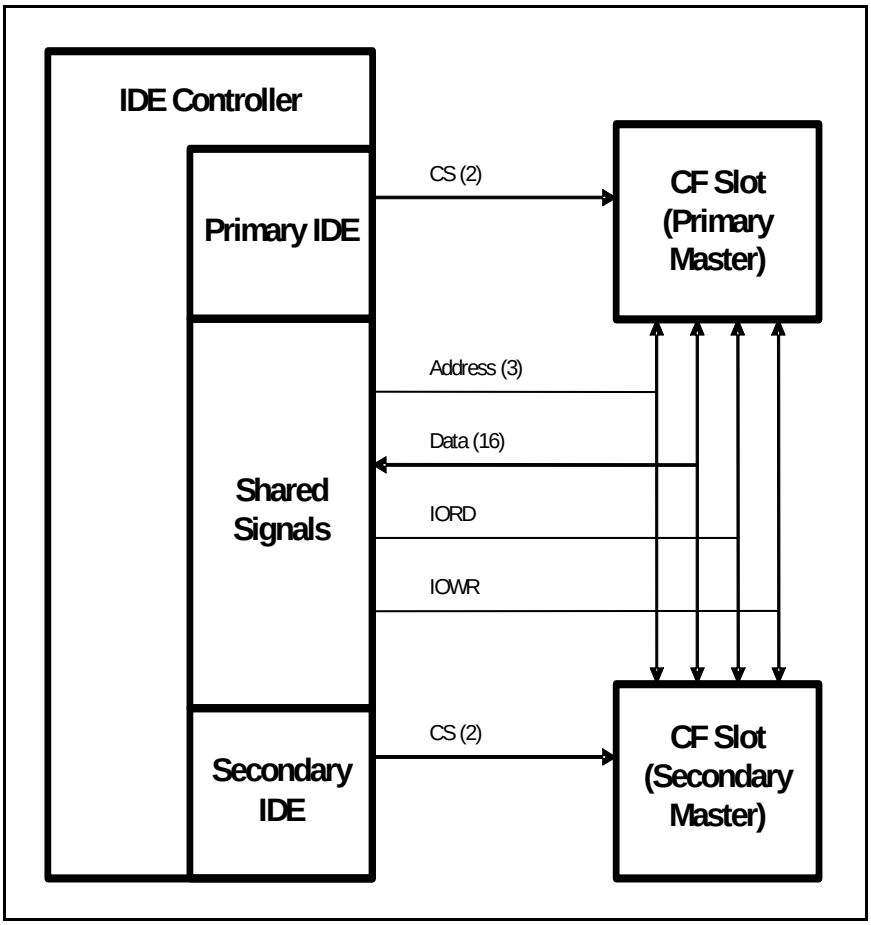

Figure 6: Common Shared Bus Configuration

Figure 7 shows another shared bus architecture. Note that the Chip Select signals are shared instead of the read/write signals. This shared bus architecture is a more questionable design in that each device is susceptible to any noise on their respective read/write signals if either of them are accessed.

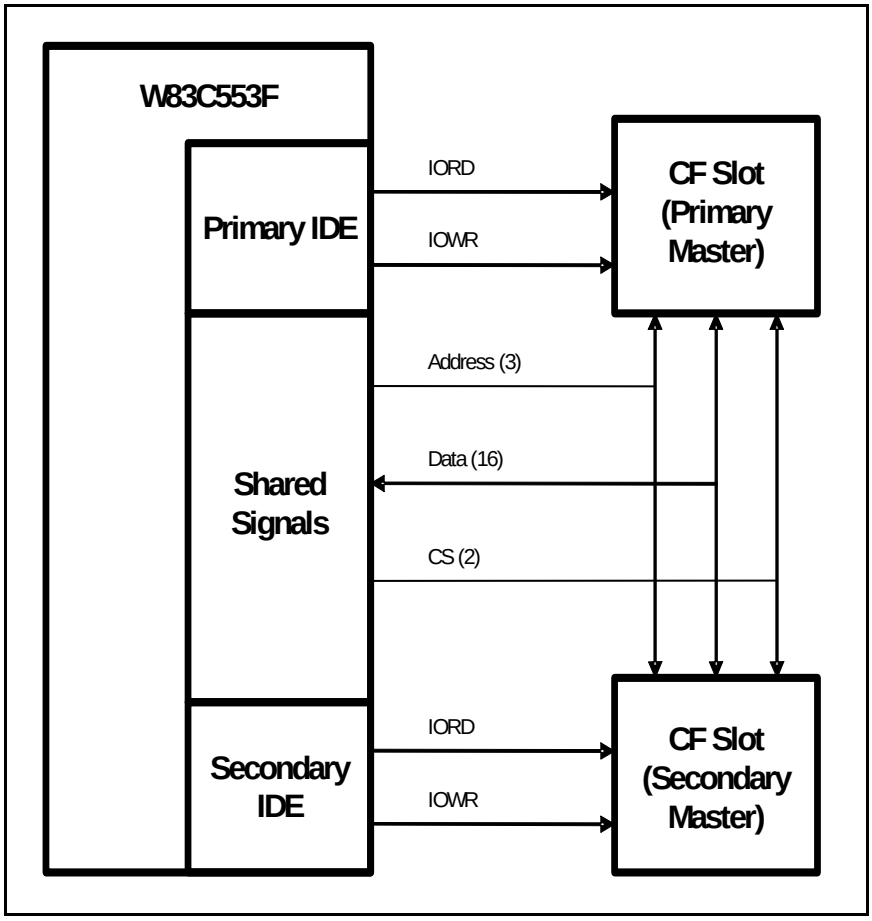

Figure 7: Unique Shared Bus Configuration

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CONSIDERATIONS WITH HIGHER SPEED INTERFACES

TRENDS

The current PATA solution requires 40 signals. The need to support higher data rates, at the same time reducing board space and providing improved data/signal integrity, has necessitated a move towards a serial data transfer strategy with differential signaling. A serial transfer would minimize the pin count on devices (in effect minimizing board space), and the differential signaling would increase the data transfer rates as well as reduce the crosstalk and noise of the transfer (in effect improving the data/signal integrity).

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Differential signaling is a method for transmitting information over a pair of wires that reduces noise on a connection by rejecting common-mode interference. One wire (D+) carries the signal and the other wire (D-) carries the inverse of the signal. At the receiver end, D- is inverted and summed with D+, which effectively cancels out the noise created across the transmission line. Although differential signaling is more noise immune than single-ended signaling, it is very sensitive to slew rate and skew — careful layout design rules must be followed.

Two such solutions are Universal Serial Bus (USB) and Serial ATA (SATA). The USB is a 480Mbps interface with a single differential pair used for data communication. Refer to the *USB 2.0 Design Guidelines* for the proper termination and PCB layout specifications. The SATA 1.0 is a 1.5Gbps interface that is similar to the USB from an electrical standpoint, except it uses two differential pairs used for data communication. The design guidelines can be found in the SATA specification.

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SUMMARY

Designs get much more complex as bus speed increases. Signals start to behave more like transmission lines. Because of this, impedance matching plays an important role that must be taken in to account for proper bus design. The following guidelines should be taken in the design development cycle:

- A true understanding of the bus specification is needed to provide the proper solution for the design.
- The best time to select termination is early in the design. If uncertain of the termination, always place 0Ω termination resistors in the design.
- Observe the signals with an oscilloscope to verify that proper termination values are used. Make adjustments to the termination values if there is excessive overshoot or over-damping.
- If preferred, use Simulation Programming with Integrated Circuits Emphasis (SPICE) modeling, which is a general purpose analog circuit simulator. SPICE is a powerful program that is used in IC and board level designs to check the signal integrity of circuit designs and predict circuit behavior.

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REFERENCES

DOCUMENTATION

- *ATA/ATAPI-5 Standards Specification*, Revision 3, February 2000
- *Serial ATA Specification*, Revision 1.0, August 2001
- *Universal Serial Bus Specification*, Revision 2.0, April 2000
- *High-Speed USB Platform Design*, Revision 1.0, July 2000

EQUIPMENT

- Tektronix Oscilloscope, P/N TDS5104B
- Tektronix Logic Analyzer, P/N TLA5202

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